Finite-Element Electromagnetic Characterization of Parasitics in Multifinger Thermally Shunted HBT's

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***Abstract*— This letter describes a methodology to extract parasitic capacitances and evaluate losses in multifinger thermally shunted heterojunction bipolar transistors (HBT's) using three-dimensional (3-D) electromagnetic modeling. This method is based on the partitioning of the structure into zones of propagation, which simplifies the analysis of the computed scattering matrices. The approach is validated using on-wafer measurements of open-circuit test structures. This letter also addresses the impact of changes in device topology on parasitic coupling capacitance and association efficiency.**

I. Introduction

LINEAR and nonlinear circuit design requires the use of accurate and reliable electrical models. In modeling microwave transistors, extrinsic parasitic elements are generally extracted using on-wafer measurements. Unfortunately, direct electrical extraction of lumped parasitic elements gives little insight into the origins of these parasitics. While not vital for circuit simulation, a more thorough analysis of the distributed nature of losses and parasitic capacitance would yield useful information for the device designer. For this reason we have developed a characterization method based on three-dimensional (3-D) finite-element electromagnetic simulations. This method is applied to the complex structure of a multifinger heterojunction bipolar transistor (HBT) with emitter thermal shunt. The thermal shunt is an electrothermal stabilization technique widely used for power HBT's [1], [2]. The technique involves placing a metallic mass over the active region of the device to lower its thermal resistance. A goal of this study is to characterize the parasitic electrical effects incurred by this technology.

II. Method

For the HBT topology shown Fig. 1, there exist different modes of propagation. We use the 3-D finite-element electromagnetic simulator HP-HFSS [3] to model the transitions between microstrip and coplanar modes (zones A and B, zones D and E) and coplanar and hybrid modes (zones B and C, zones C and D). Whereas classic analytical laws or a distributed elements approach are useful for circuit design, they fail to specify the origins of parasitic coupling capacitance for complex structures. The computed electric and magnetic field plots yield qualitative and quantitative information about the degree of electromagnetic coupling between the emitter, base, and collector metallizations as well as losses incurred by transitions in propagation modes. We have developed a technique to model coupling capacitance for complex HBT structures and to evaluate changes in device design without the need for costly device prototyping.

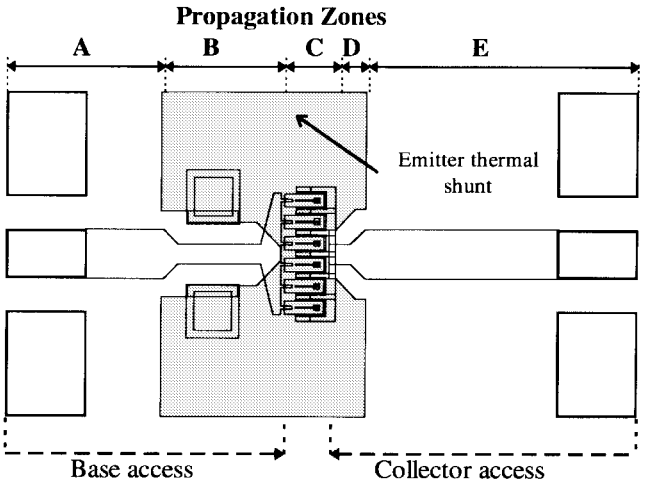

Fig. 1. Six-emitter-finger HBT layout showing zones of propagation. Shaded area is emitter thermal shunt metal.

The simulated structure is modeled as three sections: the base and collector access regions and the active device region. In the device region, we assume that the mode of propagation is fixed (hybrid), while for the base and collector access regions, there are microstrip/coplanar and coplanar/hybrid transitions in the propagation modes. To calculate useful scattering matrices, the boundaries between these regions are chosen so that they do not lie in the transition regions.

Within the active device region of the HBT, there is capacitive coupling between the base and collector metallizations and the pillar metal of the emitter thermal shunt as well as the shunt metal itself. This coupling is analyzed by simulating a thermally shunted single emitter finger with two collector and two base metallizations, situated along each side of the finger. The deembedded S-parameters are transformed into Y-parameters, which are used to compute coupling capacitance.

In analyzing the base and collector access regions of the device, we avoid fitting the computed S-parameter data to equivalent circuit representations. Instead, we use a black box representation of these access regions in our CAD circuit

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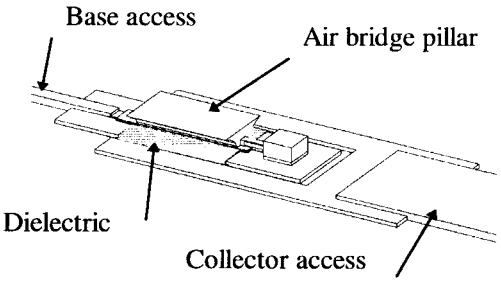

Fig. 2. Single-finger HBT active region showing emitter thermal shunt pillar metal and interlayer dielectric (shaded region).

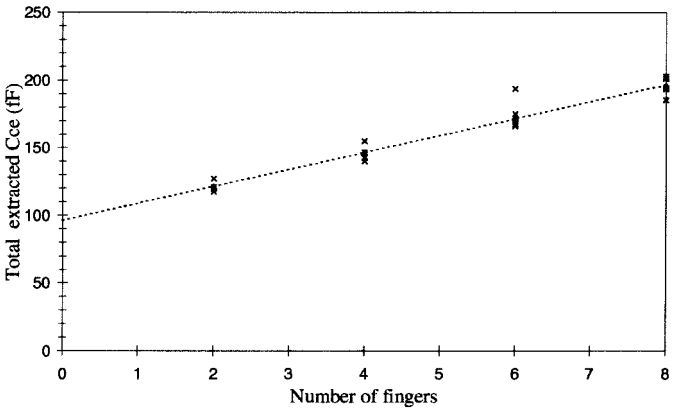

Fig. 3. 300-MHz extracted collector-emitter capacitance versus number of emitter fingers for open-circuit test structures.

design software. As will be shown, we use the calculation of association efficiency to evaluate losses in these networks.

III. Method Validation

This method has been validated by direct extraction of capacitance performed at low frequency for a wafer on which only open-circuited (i.e., passive) HBT structures have been fabricated. For comparison, we simulated the single-emitter finger HBT topology depicted in Fig. 2, which closely resembles the actual structure of the fabricated devices.

Scattering parameters were computed for reference planes sufficiently far from the device so that the propagation mode is established, and the S-parameters are deembedded at planes close to the so-called active region. At 10 GHz, coupling elements are lumped, and the admittance matrix is

$$\mathbf{Y_{ij}} = \begin{pmatrix} \text{j.w.}(\text{Cbe} + \text{Cbc}) & -\text{j.w.Cbc} \\ -\text{j.w.Cbc} & \text{j.w.}(\text{Cbc} + \text{Cce}) \end{pmatrix}.$$

To compare this model with electrical measurements, on-wafer measurements were performed on passive HBT's with up to eight emitter fingers (each $2 \times 30\ \mu\text{m}^2$) to extract coupling capacitance at low frequency ($\approx$300 MHz). The passive HBT's were fabricated on a semiinsulating substrate without active semiconductor layers. As an example, the total extracted emitter-collector capacitance is depicted in Fig. 3. From these results, we formulated a linear law

$$\text{C}_{\text{total}} = \text{C}_{\text{pad}} + (\#\ \text{fingers} \times \text{C}_{\text{coupling}}).$$

TABLE I
Simulated and Measured Coupling Capacitance for HBT Design of Fig. 1

		Cbe	Cbc	Cce
Measure	C_{pad}	78 fF	___	96.3 fF
	$C_{coupling}$	30.6 fF	4.5 fF	12.6 fF
Simulation	$C_{coupling}$	55 fF	3.8 fF	14 fF

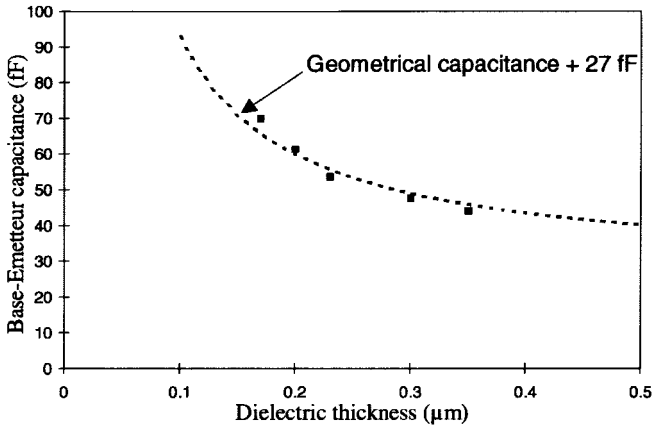

Fig. 4. Simulated base-emitter capacitance versus interlayer dielectric thickness at 10 GHz. Analytical model for geometrical capacitance (adjusted by 27 fF) included for reference.

Similar calculations were made for the base-collector and base-emitter capacitances. The results are summarized in Table I.

Note the good agreement between the measured and simulated coupling capacitance for Cbc and Cce. The variation in values for base-emitter capacitance is likely due to imprecise knowledge of the thickness of the interlayer dielectric between the base and emitter metals for the fabricated test devices. In addition the standard deviation of the measured values for base-emitter capacitance was $\pm$26% of the average value of 30.6 fF and was much larger than the variations in Cbc and Cce. This suggests a variation in the thickness of the silicon nitride interlayer dielectric.

IV. Results

We can now study the impact of changes in HBT topology on parasitic coupling. For our devices, parasitic input capacitance Cbe is proportional to the thickness of the dielectric between the base metal and the emitter pillar metal. Although Table I depicts a rather large variation between simulated and modeled base-emitter coupling capacitance, we attribute this to the lack of precise knowledge of the thickness and uniformity of the dielectric of the test structures. We assume for this study that the values given by the simulation are representative and show the correct trends as we vary thickness. The simulated influence of this thickness is presented in Fig. 4. Also shown for reference is the calculated geometric capacitance. Note that this coupling capacitance ($\text{Cbe}_{\text{coupling}}$) is not equal to the planar geometric capacitance. To compare the shapes of the two curves, it is necessary to add a capacitance of 27 fF to the geometric capacitance. This offset is likely due to radiative coupling at the edges of the metallizations. The frequency dependence of this radiative coupling has not been addressed.

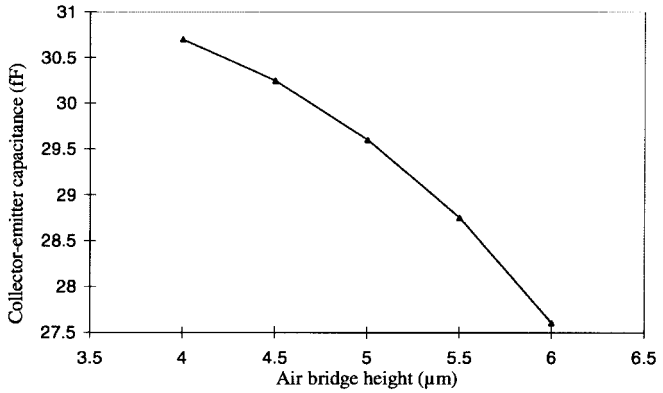

Fig. 5. Simulated collector-emitter capacitance versus spacing between collector metallization and emitter thermal shunt.

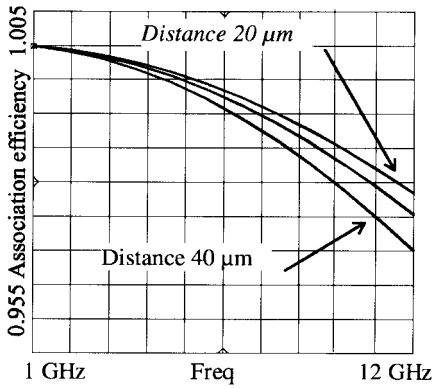

Fig. 6. Computed association efficiency for three different emitter-finger spacings (four-finger HBT).

The distance between the emitter thermal shunt and the collector metal is also an important topology variable. Fig. 5 represents the influence of this height on simulated collector-emitter capacitance. It is evident that the complex geometry of the HBT with the thermal bridge does not follow a simple planar capacitance law $(\varepsilon A/d)$.

From a thermal standpoint, it is preferable to separate emitter fingers as much as possible to minimize thermal coupling between them. This separation distance has a direct influence on the losses of the input and output access regions. The association efficiency for the input network of a four-emitter-finger device is represented Fig. 6 for emitter separations of 20, 30, and 40 μm. The association efficiency is defined as the sum of the radio frequency (RF) power injected into the input port(s) of a passive network divided by the sum of the power received by the output port(s) of a passive network. This calculation assumes 50-Ω source and load impedances. We note that losses introduced by the input network are minimized if the distance between fingers is reduced. Unfortunately, this reduction is incompatible with thermal considerations. Although a second-order effect for the four-finger device studied, we expect the effect of finger separation on association efficiency to be significant for large-area HBT's with eight or more fingers.

V. Conclusion

An extraction methodology for electrical parasitics in complex transistor topologies has been presented. The finite-element electromagnetic software HFSS is used to compute scattering matrices for the input–output access regions and the active device region. With this method it is possible to localize the origins of coupling parasitics and develop solutions to minimize them. In optimizing the high-frequency behavior of the passive regions of proposed microwave transistor designs, one can avoid costly design prototyping.

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